Frederic Sala

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Education

2013-2016 Ph.D. in Electrical Engineering, University of California, Los Angeles (UCLA)
Dissertation: "Algorithms and Coding Techniques for Reliable Data Management and Storage"
(Outstanding Ph.D. Dissertation Award - Signals & Systems Track)
GPA: 4.0/4.0

2011-2013 M.S. in Electrical Engineering, University of California, Los Angeles (UCLA)
Thesis: "Novel Coding Strategies for Multi-Level Non-Volatile Memories"
(Outstanding M.S. Thesis Award - Signals & Systems Track)
GPA: 4.0/4.0

2006-2010 B.S. in Electrical Engineering, University of Michigan, Ann Arbor
Summa Cum Laude

Research interests

Problems related to machine learning, statistical inference, information and coding theory. In particular, analysis and design of algorithms that must operate on unreliable data. How to

- design algorithms that can tolerate unreliable input data,
- protect data from noise and uncertainty,
- reliably store data on unreliable hardware,
- reconstruct/reconcile data that has already been modified or corrupted.

Techniques based on algorithms, statistical inference, information and coding theory, optimization, combinatorics.

Honors & awards

2017 Outstanding Ph.D. Dissertation Award
UCLA Department of Electrical Engineering (Signals & Systems Track)

2015-2016 UCLA Dissertation Year Fellowship

2015 Qualcomm Innovation Fellowship Finalist

2013 Edward K. Rice Outstanding Masters Student Award
UCLA Henry Samueli School of Engineering & Applied Science

2013 Outstanding M.S. Thesis Award
UCLA Department of Electrical Engineering (Signals & Systems Track)

2012-2015 **National Science Foundation Graduate Research Fellowship (NSF GRFP)**

2011-2012 UCLA Graduate Fellowship

2006-2010 University of Michigan Shipman Society Scholarship
2006-2010 University of Michigan Engineering Scholarship of Honor

Publications & talks

Books and monographs

2016 L. Dolecek and **F. Sala**, "Channel coding methods for non-volatile memories," *Foundations and Trends in Communications and Information Theory*, vol. 13, no. 1, pp. 1-136, Feb. 2016.

Journal articles

2017 **F. Sala**, C. Schoeny, R. Gabrys, and L. Dolecek, "Exact reconstruction from insertions in synchronization codes," *IEEE Transactions on Information Theory*, vol. 63, no. 4, pp. 2428-2445, Apr. 2017.

2017 **F. Sala**, C. Schoeny, S. Kabir, D. Divsalar, and L. Dolecek "On nonuniform noisy decoding for LDPC codes with application to radiation-induced errors," *IEEE Transactions on Communications*, vol. 65, no. 4, pp. 1438-1450, Apr. 2017.

2016 **F. Sala**, N. Bitouze, C. Schoeny, and L. Dolecek, "Synchronizing files under a large number of edits," *IEEE Transactions on Communications*, vol. 64, no. 6, pp. 2258-2273, Jun. 2016.

2016 R. Gabrys, E. Yaakobi, F. Farnoud, **F. Sala**, S. Bruck, and L. Dolecek, "Codes correcting erasures and deletions for rank modulation," *IEEE Transactions on Information Theory*, vol. 62, no. 1, pp. 136-150, Jan. 2016.

2015 L.F. Wanner **et al.**, "NSF expedition on variability-aware software: Recent results and contributions," *Information Technology*, vol. 57, no. 3, pp. 181-198, Jun. 2015.

2015 **F. Sala**, K.A.S. Immink, and L. Dolecek, "Error control schemes for modern Flash memories: solutions for Flash deficiencies," *IEEE Consumer Electronics*, vol. 4, no. 1, pp. 66-73, Jan. 2015.

2014 R. Gabrys, **F. Sala**, and L. Dolecek, "Coding for unreliable Flash memory cells," *IEEE Communication Letters*, vol. 18, no. 9, pp. 1491-1494, Jul. 2014.

2013 **F. Sala**, R. Gabrys, and L. Dolecek, "Dynamic threshold schemes for multi-level non-volatile memories," *IEEE Transactions on Communications*, vol. 61, no. 7, pp. 2624-2634, Jul. 2013.

2010 E. Cheng, L. Liptak, and **F. Sala**, "Linearly many faults in 2-tree generated networks," *Networks*, vol. 55, no. 2, pp. 90-98, Mar. 2010.

Conference publications

2017 **F. Sala**, S. Kabir, G. V. d. Broeck, and L. Dolecek, "Don't fear the bit flips: optimized coding strategies for binary classification," submitted, 2017.

2016 K. Mazooji, **F. Sala**, G. V. d. Broeck, and L. Dolecek, "Robust channel coding strategies for machine learning data," in *Proc. IEEE 54th Allerton Conference on Communication, Control, and Computing*, Monticello, IL, Sept. 2016.

2016 **F. Sala**, H. Duwe, L. Dolecek, and R. Kumar, "A unified framework for error correction techniques in on-chip memories," presented at *Workshop on Silicon Errors in Logic - System Effects (SELSE-12)*, Austin, Texas.
Best of SELSE-12 paper, presented in special session at *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, Toulouse, 2016.

2016 **F. Sala**, R. Gabrys, C. Schoeny, K. Mazooji, and L. Dolecek, "Exact sequence reconstruction for insertion-correcting codes," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Barcelona, 2016.

2015 **F. Sala**, C. Schoeny, D, Divsalar, and L. Dolecek, "Asymmetric ECCs for Flash in high radiation environments," in *Proc. IEEE Asilomar Conference on Signals, Systems and Computers,* Monterey, CA, 2015 (invited).

2015 **F. Sala**, C. Schoeny, D. Divsalar, and L. Dolecek, "Asymmetric error-correcting codes for Flash memories in high-radiation environments," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Hong Kong, 2015.

2015 C. Schoeny, **F. Sala**, and L. Dolecek, "Analysis and coding schemes for the Flash Normal-Laplace mixture channel," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Hong Kong, 2015.

2015 **F. Sala**, C. Schoeny, R. Gabrys, and L. Dolecek, "Three novel combinatorial theorems for the insertion/deletion channel," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Hong Kong, 2015.

2014 **F. Sala**, R. Gabrys, and L. Dolecek, "Gilbert-Varshamov-like lower bounds for deletion-correcting codes," in *Proc. IEEE Information Theory Workshop (ITW)*, Hobart, Australia, 2014.

2014 **F. Sala**, R. Gabrys, and L. Dolecek, "Deletions in multipermutations," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Honolulu, Hawaii, 2014.

2014 R. Gabrys, E. Yaakobi, F. Farnoud, **F. Sala**, J. Bruck, and L. Dolecek, "Single-deletion-correcting codes over permutations," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Honolulu, Hawaii, 2014.

2013 N. Bitouze, **F. Sala**, S. M. S. Tabatabaei, and L. Dolecek, "A practical framework for efficient file synchronization," in *Proc. IEEE 51st Allerton Conference on Communication, Control, and Computing*, Monticello, IL, Oct. 2013.

2013 **F. Sala** and L. Dolecek, "Constrained rank modulation," in *Proc. IEEE Information Theory Workshop (ITW)*, Sevilla, Spain, Sept. 2013.

2013 **F. Sala** and L. Dolecek, "Counting sequences obtained from the synchronization channel," in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Istanbul, Turkey, July 2013.

2012 **F. Sala**, R. Gabrys, and L. Dolecek, "Dynamic threshold schemes for multi-level nonvolatile memories," in *Proc. IEEE Asilomar Conference on Signals, Systems and Computers*, Monterey, CA, Nov. 2012.

Book chapters

2016 **F. Sala**, C. Schoeny, and L. Dolecek, "Advanced algebraic and graph-based ECC schemes for Flash memories," in *3D Flash Memories*, Rino Micheloni, Ed. Springer, 2016, pp. 321-348.

Theses

2016 **F. Sala**, "Algorithms and Coding Techniques for Reliable Data Management and Storage." Ph.D. Dissertation, University of California, Los Angeles, December 2016.

2013 **F. Sala**, "Novel Coding Strategies for Multi-Level Non-Volatile Memories." M.S. Thesis, University of California, Los Angeles, May 2013. Distinguished M.S. Thesis Award - Signals & Systems Track

Talks

2016 **F. Sala**, "Error-correcting codes for radiation-induced error patterns in flash memories," Non-Volatile Memories Workshop (NVMW), San Diego, CA, March 7, 2016.

2016 **F. Sala**, "Exact reconstruction of coded data from traces." Graduation Day Talk at Information Theory and Applications Workshop (ITA), La Jolla, CA, February 3, 2016.

2014 **F. Sala**, "Constrained rank modulation for flash memories," Non-Volatile Memories Workshop (NVMW), San Diego, CA, March 11, 2014.

2013 **F. Sala**, "Reducing energy usage through a novel file synchronization algorithm," DIMACS Workshop on Algorithms for Green Data Storage, Rutgers University, New Brunswick, NJ, December 18, 2013.

2013 **F. Sala**, "Dynamic threshold schemes for multi-level non-volatile memories," Non-Volatile Memories Workshop (NVMW), San Diego, CA, March 5, 2013.

Industry experience

2015 Samsung Electronics, Research Engineering Intern
Memory Systems Laboratory (MSL) - New Memory Technologies Group

2014 Jet Propulsion Laboratory (JPL), Research Engineering Intern
Information Processing Group

2010-2011 Microsoft Corporation, Software Development Engineer
Windows Phone Group

2009 Microsoft Corporation, Software Development Engineer Intern
Zune/Xbox 360 Group

2008 Microsoft Corporation, Software Development Engineer Intern
Windows Ehome Group

Relevant courses

Engineering

Information Theory	Channel Coding
Data Networks	Inference and Estimation
Circuit Analysis	Signals and Systems
Logic Design	Digital Signal Processing
Computer Organization	DSP Design Laboratory

Mathematics

Probability	Stochastic Processes
Real Analysis	Differential Equations
Combinatorics	Abstract Algebra
Linear Programming	Convex Programming
Linear Algebra	Graph Theory
Number Theory	Algebraic Number Theory

Skills

Computing Languages: C#, C++, Verilog hardware description language
Engineering Applications: MATLAB, Mathematica, LaTeX typesetting language